

## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method, comprising:  
  
retrieving an instruction from a memory unit;  
  
partially pre-decoding the instruction at a direct memory access unit; ~~and~~  
  
providing the pre-decoded instruction from the direct memory access unit to a processing element;;  
  
• completely decoding the pre-decoded instruction at the processing element; and  
  
executing the completely decoded instruction at the processing element.
2. (original) The method of claim 1, wherein said providing comprises storing the pre-decoded instruction in memory local to the processing element.
- 3-4. (canceled)
5. (original) The method of claim 1, further comprising:  
  
loading instructions into the memory unit during a boot-up process.
6. (original) The method of claim 1, wherein the processing element is a reduced instruction set computer device.

7. (original) The method of claim 6, wherein the pre-decoded instruction comprises execution control signals.

8. (currently amended) An apparatus, comprising:

an input path to receive an instruction from a memory unit;

a direct memory access unit including an instruction pre-decoder to partially pre-decode the instruction; ~~and~~

an output path to provide a partially pre-decoded instruction from the direct memory access unit ~~to a processing element ; and~~

a processor to receive the partially pre-decoded instruction and completely decode the partially pre-decoded instruction.

9. (original) The apparatus of claim 8, further comprising:

the memory unit coupled to the input path.

10. (canceled)

11. (currently amended) The apparatus of claim [10] 8 , wherein the processing element includes a local memory to store the pre-decoded instruction.

12. (currently amended) The apparatus of claim [10] 8 , including a plurality of processing elements, each processing element being associated with a direct memory access unit that includes an instruction pre-decoder.

13. (currently amended) The apparatus of claim [10] 8 , wherein the input path has  $n$  bits, the output path has  $q$  bits, and  $n < q$ .

14. (currently amended) The apparatus of claim [10] 8 , wherein the direct memory access unit, the memory unit, and the processing element are formed on an integrated circuit.

15. (currently amended) The apparatus of claim [10] 8 , wherein the processing element is a reduced instruction set computer device having an instruction pipeline.

16. (currently amended) An article, comprising:

a computer-readable storage medium having stored thereon instructions that when executed by a machine result in the following:

retrieving an instruction from a memory unit,

partially pre-decoding the instruction at a direct memory access unit, and

providing the pre-decoded instruction from the direct memory access unit to a processing element to be completely decoded.

17. (original) The article of claim 16, wherein said providing comprises storing the pre-decoded instruction in memory local to the processing element.

18. (currently amended) An apparatus, including:

a global memory to store instructions;

an instruction pre-decoder; and

a processor, wherein the instruction pre-decoder is to partially pre-decode an instruction as it is being transferred from the global memory to the processor, wherein the processor is to completely decode a partially pre-decoded instruction.

19. (currently amended) The apparatus of claim 18, further comprising:

a direct memory access unit to arrange for the instruction to be retrieved from the global memory unit and to arrange for a partially pre-decoded instruction to be provided to the processor.

20. (original) The apparatus of claim 18, wherein a pre-decoded instruction comprises execution control signals.

21. (currently amended) A system, comprising:

a multi-directional antenna; and

an apparatus having a direct memory access unit that includes:

an input path to receive an instruction from a memory unit,  
an instruction pre-decoder to partially pre-decode the instruction, and  
an output path to provide a pre-decoded instruction ~~to a processing element ; and~~  
a processor to receive and completely decode the partially pre-decoded instruction.

22. (original) The system of claim 21, wherein the apparatus is a digital base band processor.

23. (original) The system of claim 22, wherein the digital base band processor is formed as a system on a chip.

24. (original) The system of claim 21, wherein the system is a code-division multiple access base station.